Hybrid Photonic Plasmonic Interconnects: Low Latency Energy-and-Area-Efficient On-Chip Interconnects

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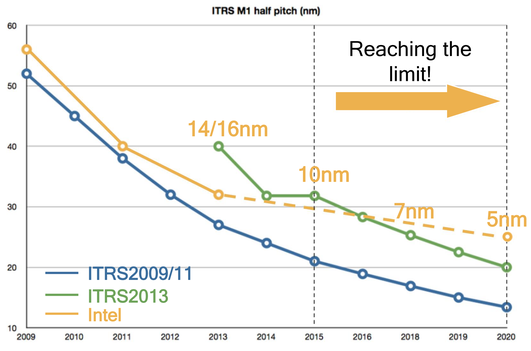
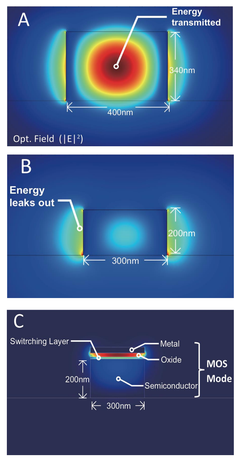
Motivation

- Moore's Law for traditional electric integrated circuits is facing challenges.
- The requirement of electronic device down-scaling has led to severe limitations.
- The available bandwidth per compute continues to drop and will likely reach its end at 5 nm technology node according to the 2013 ITRS.
- The increasing demand for data movement, requires novel interconnect technologies over classical electronic links, particularly in terms of latency, energy efficiency and integration.



Photonics

- ☒ Diffraction Limited (> λ/2)
- ☒ Large Footprint (μm² ~ mm²)
- ☒ Low LMI → High Power (pJ)
- ☑ Long Propagation (cm)



Plasmonics

- ☑ No Diffraction Limit (< λ/2)
- ☑ Area Efficient (nm² ~ μm²)
- ☑ Energy Efficient (fJ)
- ☒ Short Propagation (μm)

Hybrid

- ☑ High LMI→ Low Power
- ☑ High Scaling
- ☑ High Bit Density
- ☑ Long Range

Passive device → Light Propagation
Active device → Light Modulation

Hybrid Photonic Plasmonic Interconnects (HyPPIs) strategy combines photonics with plasmonic interconnect technology and improves link performance in two ways:

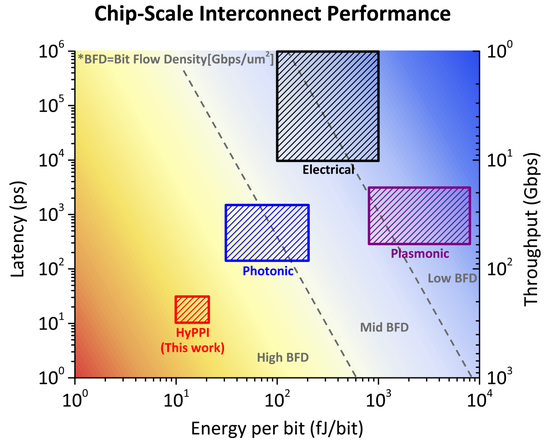
HyPPI – Extrinsic: The diffraction-limited photonic devices are replaced with plasmonic counterparts, but keep the low-loss SOI platform as the passive backbone.

HyPPI – Intrinsic: Direct light source modulation with electrical drivers and bypassing the electro-optic modulator.

Abstract

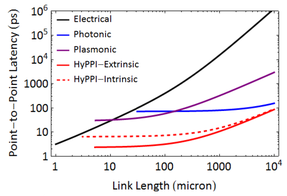
We benchmark electrical, photonic, and plasmonic options and contrast them with Hybrid Photonic Plasmonic Interconnects (HyPPIs) where we consider plasmonics for active manipulation devices, photonics for passive propagation integrated circuit elements with two modulation strategies. Our analysis shows that such hybridization shows superiority in:

- Point-to-point Latency
- Throughput
- Crosstalk Length
- Energy Efficiency
- Energy-Delay Product
- Bit Flow Density (BFD)
- Capability-to-Latency-Energy-Area Ratio (CLEAR)

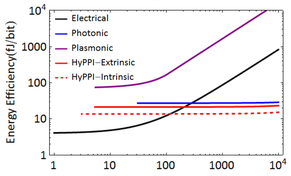


Link Performance

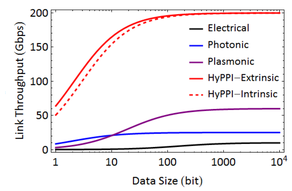
Point-to-point latency: is defined as the time a single bit of data packet requires to travel from the sender to the receiver.



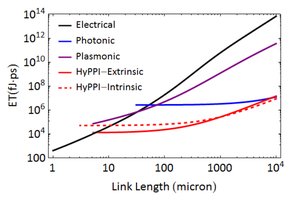
Energy Efficiency: includes the energy cost by all the devices on the link, such as lasers, modulators, detectors with related drivers and waveguide loss.



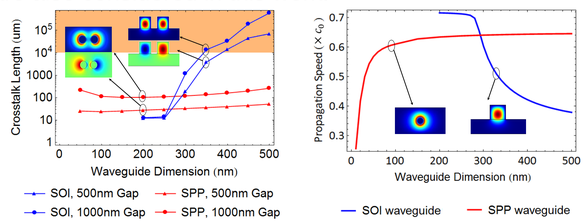
Link Throughput: is defined as the number of bits a medium can deliver in a given time period, which related to the data size, channel capacity and point-to-point latency.



Energy Delay Product: is the product of the first two FOMs and can be used to optimize the weighted energy consumption and system latency simultaneously.



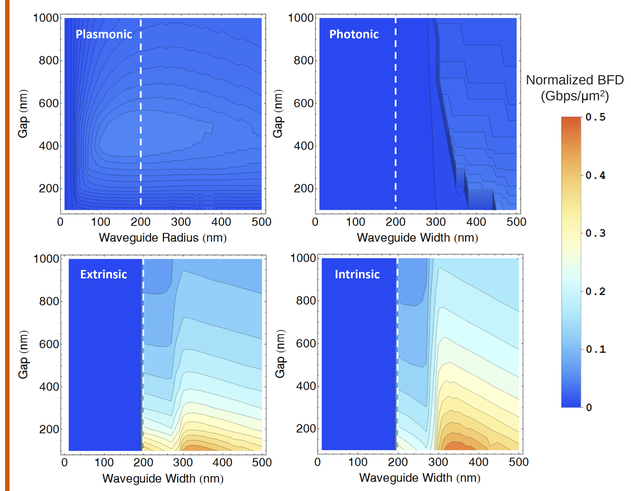
Crosstalk Length and Prop. Speed: is the link length where the energy leakage is 25% from one waveguide to its adjacent neighbor and the propagation speed for different waveguide dimensions are also considered in this work.



Bit Flow Density

Bit Flow Density (BFD) is the number of bits transmitted through a certain chip width (cross-section) to reach a specific required communication range (chip length). It combines the major performances, such as link latency, overall throughput and link crosstalk, and highly related to the size of each device and spacing.

$$BFD = \frac{Total\ Throughput}{Chip\ area} = \frac{\#\ Links \times Throughput\ per\ Link}{Chip\ length \times Chip\ width}$$



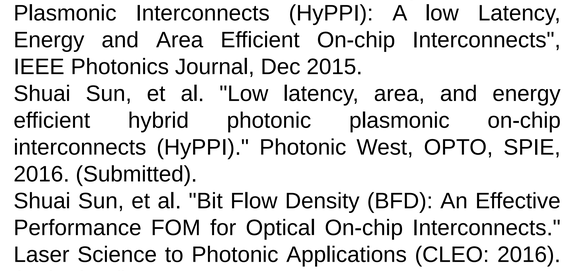
- Plasmonic interconnects achieve the highest value in the center of its plot, indicating that plasmonic links are only able to provide high BFD over chip scales with smaller waveguide diameter and medium gaps.
- For both photonic and HyPPI links, the high BFD regions are correlated with both low crosstalk (large waveguide width) and dense waveguide integration (waveguide gap).
- Photonic interconnect and HyPPI shows low BFD below 200 nm waveguide widths due to the light diffraction limit of the SOI waveguide.

CLEAR

In Capability-to-Latency-Energy-Area Ratio (CLEAR), capacity and distance, on the numerator, are the two capabilities that represent the number of bits and the distance that the channel can send. The denominator has all related factors that will reduce the overall performance for the link. Therefore, this FOM favors the technology with higher bit rate with lower latency, energy and area cost and able to deliver the data through longer distances.

$$CLEAR = \frac{Capability}{Cost \times Power} = \frac{Capacity \times Distance}{Latency \times Energy \times Area}$$

$$= \frac{Gbps \times \mu m}{psec \times {fJ}/{bit} \times \mu m^2}$$



Results

HyPPI hybridizes photonic with plasmonic interconnects to provide a point-to-point link that shows significant improvements in performance relative to that of pure photonic or pure plasmonic links in:

- ✓ P2P latency (< 100 ps/cm)
- ✓ Energy (< 20 fJ/bit)
- ✓ Link throughput (> 200 GHz)
- ✓ Communication length (> 1 cm)
- ✓ Bit Flow Density (0.1 ~ 0.5 Gbps/μm², 1 ~ 3 orders higher than other interconnect options)
- ✓ Broader CLEAR range (30 μm ~ 1 cm) which makes up the short range of electrical interconnect (< 30 μm)

Related Works

- Shuai Sun, et al. "Photonic-Plasmonic Hybrid Interconnects: a Low-latency Energy and Footprint Efficient Link." IPR, OSA, 2015.
- Shuai Sun, et al. "The Case for Hybrid Photonic Plasmonic Interconnects (HyPPI): A low Latency, Energy and Area Efficient On-chip Interconnects", IEEE Photonics Journal, Dec 2015.
- Shuai Sun, et al. "Low latency, area, and energy efficient hybrid photonic plasmonic on-chip interconnects (HyPPI)." Photonic West, OPTO, SPIE, 2016. (Submitted).
- Shuai Sun, et al. "Bit Flow Density (BFD): An Effective Performance FOM for Optical On-chip Interconnects." Laser Science to Photonic Applications (CLEO: 2016). (Submitted).